Remarks

Reconsideration as well as allowance of the above-identified application, as currently amended, is respectfully requested.

By the above-made amendments, claims 1-24 are now pending of which claims 1-19 stand withdrawn, claim 20 is currently amended and claims 23-24 are newly presented.

The amendments made to the claims are in consideration of clarifying the subject matter set forth therein including in a manner which is defining over the teachings of Ikeda, et al. (U.S. Patent No. 4,890,148), which was cited in the outstanding rejection.

The invention according to amended claim 20 is a semiconductor integrated circuit device setting forth a semiconductor substrate and a plurality of static random access memory (SRAM) cells which are disposed on the semiconductor substrate, in which each SRAM cell has a pair of n-channel drive MISFETs, a pair of p-channel load MISFETs and a pair of n-channel selection MISFETs, wherein the drive as well as the selection MISFETs contain a lightly doped drain (LDD) structure, respectively, each of the p-channel load MISFETs has a source, a drain and a gate electrode in which the drain thereof is formed inside the semi-conductor substrate, and wherein the p-channel load MISFETs contain a single drain structure, respectively.

Claim 21 (dependent on claim 20) further characterizes the two inverter circuit construction corresponding to each of the SRAM cells, e.g., each such SRAM cell is constructed as what is referred to in the specification as a 6-MIS type memory cell or a complete CMIS (complementary metal insulator semiconductor) type memory cell. An example of such a 6-MIS type memory cell construction, i.e., in which the drive and load MISFETs are configured as a pair of cross-connected inverter circuits, in which the load MISFETs are p-channel type and in which the drains thereof are formed inside the semiconductor substrate, are shown in connection with example Fig. 9, 11 and 16 of the

drawings, etc., although not limited thereto. As can be seen from Fig. 16, the p-channel load MISFET QL2 (QL2) has a drain region (4) that is formed inside the substrate (P-well) and the selection (or transfer) MISFET Qt2 (or Qt1) contains a LDD structure. *Silicide* films 7 affect improvement in the electrical contact.

Newly added dependent claim 23 further limits the substrate to one comprised of a single crystal silicon layer in which the drain of the p-channel load MISFETs are formed therein, respectively. Newly added dependent claim 24 further characterizes the semiconductor IC device to a construction in which the drain of the respective p-channel load MISFETs may be positioned under the gate electrodes thereof.

Claims 20-22 stand rejected under 35 U.S.C. 102(b) as anticipated Ikeda et al. ('148). It is submitted, however, the invention according to independent claim 20 and further according to the corresponding dependent claims thereof, as currently amended, was neither disclosed or suggested in view of Ikeda ('148). Therefore, insofar as presently applicable, the rejection is traversed and reconsideration and withdrawal of the same is respectfully requested.

Ikeda, et al. ('148) discloses a SRAM cell construction which features self-biased resistance elements (e.g., R_1 and R_2 are the load elements of the cross-connected inverters of the individual SRAM cell). This is shown with regard to Fig. 1 in Ikeda et al. ('148) (see column 4, lines 1-5). Such memory cell circuit construction in which the inverter circuit loads thereof employ, for example, polysilicon resistances are called a four (4)-MIS type memory cell. With regard to Ikeda, et al. ("148), the load resistances R_1 and R_2 of the SRAM cell are self-biased and are formed from a polycrystalline silicon film such as polycrystalline silicon layer 14 in Fig. 10 in Ikeda, et al., in which the polycrystalline silicon layer is formed on an insulator film 12. (Column 8, lines 45-56, in Ikeda, et al. '148.) Regarding Fig. 10 in Ikeda, et al. ('148), the load resistances are formed of doped polycrystalline silicon material insulatedly above the semiconductor substrate, in clear

contradistinction with that according to independent claim 20 and further according to the corresponding dependent claims thereof.

According to claims 20+ the invention sets forth a SRAM cell construction which, as noted above, can be referred to as a six (6)-MIS type memory cell or a complete CMIS (complementary metal insulator semiconductor) type memory cell, since all of the active elements associated therewith are MISFETs, including a pair of n-channel drive MISFETs, a pair of p-channel load MISFETs and a pair of n-channel selection MISFETs. The circuit configuration may be as that shown with regard to Figs. 9, 11, etc. According to independent claim 20, moreover, the device construction calls for the SRAM cells to be disposed on the semiconductor substrate in the manner in which, also, the drain of each of the P-channel load MISFETs is formed inside the semiconductor substrate. Such, it is submitted, was neither disclosed or suggested in view of Ikeda, et al. ('148) (see the above discussion as well as the device construction of Ikeda et al.'s SRAM cell shown in Figs. 3 and 10 thereof). The further limiting aspects according to newly added claims 23 and 24, it is submitted, were also neither disclosed or suggested from Ikeda, et al. ("148). For the same or similar reasons the invention according to claims 21 and 22, both of which are dependent claim 20, are likewise defining over the teachings of Ikeda, et al. ("148).

In a six (6)-MIS type memory cell construction, a gate induced drain leakage (GIDL) current becomes the predominant leakage current in the data-holding state (e.g. see the discussion from page 18, line 17, to page 19, line 11, of the substitute specification). It is submitted, the invention according to claims 20-24 covers a device construction to achieve such GIDL current reduction. Ikeda, et al. ('148), however, taught a construction (e.g., see Figs. 3 and 10) away from that, i.e., a memory cell construction in connection with the preventing of soft errors such as attributed to alpha particle radiation.

Therefore, in view of the amendments presented hereinabove together with these accompanying remarks, reconsideration as well as withdrawal of the outstanding rejection and early allowance above-identified application is respectfully requested.

To the extent necessary, applicants petition for an extension of time under 37 CFR §1.136. Please charge any shortage in the fees due in connection with the filing of this paper, including Extension of Time fees, to the Deposit Account of Antonelli, Terry, Stout & Kraus, LLP, Dep. Acct. No. 01-2135 (501.40147CX2), and please credit any excess fees to such deposit account.

Respectfully submitted,

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